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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,632	07/28/2003	Takanori Saei	Q76734	4316

7590 04/03/2006

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EXAMINER

TON, MY TRANG

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/627,632

Applicant(s)

SAEKI, TAKANORI

Examiner

My-Trang N. Ton

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 60-73 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 60-73 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/330,162.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.


MY-TRANG NUTON
PRIMARY EXAMINER

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "said first terminal being coupled to said first and second nodes of said first unit circuit and said first node of said second unit circuit, said second terminal being coupled to said first and second nodes of said third unit circuit and said second node of said second unit circuit, and said first, second and third output terminals being coupled respectively to the third node of said first unit circuit, the third node of said second unit circuit and the third node of said third unit circuit" (last 7 lines of claim 67) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

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application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

Claims 67-73 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 67, the limitation "said first terminal being coupled to said first and second nodes of said first unit circuit and said first node of said second unit circuit, said second terminal being coupled to said first and second nodes of said third unit circuit and said second node of said second unit circuit, and said first, second and third output terminals being coupled respectively to the third node of said first unit circuit, the third node of said second unit circuit and the third node of said third unit circuit" (last 7 lines of claim 67) is misdescriptive of the present invention since such limitation is not seen as recited therein. In order to avoid any confusion, Applicant is required to particularly point out how this limitation reads on the circuit arrangement of the drawings.

Moreover, claim 67 recites the limitations "said first terminal" in line 15 and "said second terminal" in line 16. There is insufficient antecedent basis for these limitations in the claim.

Claims 68-73 are rendered indefinite by the deficiencies of claim 67.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 66 is rejected under 35 U.S.C. 102(e) as being anticipated by Horiguchi et al (U.S Patent No. 5,955,896).

Horiguchi et al disclose in Fig. 16 a conventional pre-decoder including:

a first input terminal supplied with a first signal (BiB), a second input terminal supplied with a second signal (BjT), a first output terminal (CijO), a second output terminal (Cij2), a third output terminal (Cij3), and a timing control circuit (99a, 99c, 99d) coupled to said first and second input terminals (BiB, BjT) and the first, second and third output terminals (CijO, Cij2, Cij3) to produce at the first output terminal (CijO) a first output signal relative to said first input signal (BiB), at the third output terminal (Cij3) a third output signal relative to the second input signal (BjT) and at the second output terminal (Cij2) a second output signal that has a level changing edge (High or Low) appearing between a level changing edge (High or Low) of the first output signal (CijO) and a level changing edge (High or Low) of the third output signal (Cij3) (when BiB and BjT at High level, the outputs Cij0, Cij2, Cij3 will be at 1, thus, under broadest

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reasonable interpretation, Cij2=1 will be between Ci0=1 and Cij3=1) as recited in claim 66.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 60-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han et al (U.S Patent No. 5,617,043).

Han disclose in Fig. 5 a data output buffer including: a first switch (38) rendered conductive and non-conductive in response to a first signal (31); a second switch (42) rendered conductive and non-conductive in response to a second signal (33) and a third switch (40 or 44) rendered conductive when each of said first and second switches (38, 42) is rendered non-conductive. However, this reference does not specifically shown "a capacitor" recited in claim 60.

Nevertheless, it is notoriously well-known in the art that for filtering the noise, preventing breakdown in the circuit or delaying purposes by insert a capacitor at the output. Therefore, it would have been obvious at the time the invention was made for one skilled in the art to insert the capacitor at the output (connected to 39 of Han) for the purpose of filtering the noise, preventing breakdown in the circuit or delaying purposes.

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Regarding claim 61: the first signal (31 via 30) is different in phase from the second signal (33).

Regarding claim 62: a logic gate (30-36 and 58) supplied with the first and second signals (31, 33) to produce a third signal (signal applied to 44), the third switch (i.e, 44) being rendered conductive and non-conductive in response to the third signal (signal applied to 44).

Regarding claim 63: the logic gate comprises a NOR gate (36).

Regarding the limitation "a buffer circuit" recited in claim 64, it is old and notoriously well known in the art that the buffer is used as buffering or signal inverting purposes. Therefore, it would have been obvious at the time the invention was made for one skilled in the art to incorporate a buffer to the output 39 of Han for buffering or level inverting purposes.

Regarding claim 65: first switch comprises a first transistor (38) coupled between a first voltage node (VCC) and a circuit node (39), the second switch comprising a second transistor (42) coupled in parallel to the first transistor (38), the third switch comprising a third transistor (40 or 44) coupled between the circuit node (39) and a second voltage node (Ground). The same motivation applied to claim 60 is applied to claim 65 for "the capacitor" limitation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



My-Trang N. Ton
Primary Examiner
Art Unit 2816

March 30, 2006